A clean set of claims is presented below, a comparison of such claims with the pervious claims as attached.

1. (Amended) A microprocessor interface disposed between a main memory and a microprocessor, such interface comprising:

a semiconductor integrated circuit having formed therein:

(i) a data rebuffering section adapted to couple data from a one of a plurality of bi-directional data ports to a bi-directional data port of the microprocessor selectively in accordance with a control signal; and

(ii) a main memory interface adapted for coupling to the main memory for the microprocessor, such main memory interface being coupled to the data rebuffering section for providing control signals to the main memory for enabling data transfer between the main memory and the microprocessor through the data rebuffering section.

2. The microprocessor interface recited in claim 1 wherein the main memory is a selected one of a plurality of memory types each type having a different data transfer protocol and wherein the main memory interface is configured in accordance with the selected one of the plurality of memory types to provide a proper memory protocol to data being transferred between the microprocessor and the main memory through the main memory interface.

3. The microprocessor interface recited in claim 2 wherein one main memory type is an SDRAM.

4. The microprocessor interface recited in claim 2 wherein one main memory type is a RDRAM.

5. The microprocessor interface recited in claim 1 including a second integrated circuit adapted for controlling the first- mention integrated circuit, such second integrated circuit having thereon a controller adapted for coupling to the main memory interface, such controller being adapted to produce a main memory access control signal, and wherein:

the main memory has a two portions of addressable locations, one portion being addressed by the main memory interface in response to a preselected range of memory location addresses provided by the microprocessor and the other portion being addressed by the main memory interface in response to the memory access control signal provided by the

controller.

6. (Amended) The microprocessor interface recited in claim 1 wherein the data rebuffering section includes:

a selector responsive to the control signal for coupling data between a selected one of the bi-directional data ports and the bi-directional data port of the microprocessor.

7. The microprocessor interface recited in claim 1 wherein the data rebuffering section includes:

a selector responsive to the control signal for coupling the bi-directional data port of the microprocessor to either: a selected one of the bi-directional data ports; or, the main memory, selectively in accordance with the control signal.

8. (Amended) The microprocessor interface recited in claim 6 wherein the data rebuffering section includes a data distribution unit having a plurality of ports each one of the ports being coupled to a corresponding one of:

(i) the selector;
(ii) a random access memory;
(iii) an interrupt request controller;
(iv) the microprocessor; and
(v) the main memory interface.

9. The microprocessor interface recited in claim 8 wherein the main memory is a selected one of a plurality of memory types each type having a different data transfer protocol and wherein the main memory interface is configured in accordance with the selected one of the plurality of memory types to provide a proper memory protocol to data being transferred between the microprocessor and the main memory through the main memory interface.

10. The microprocessor interface recited in claim 9 wherein one main memory type is an SDRAM.

11. The microprocessor interface recited in claim 9 wherein one main memory type is a RDRAM.

12. The microprocessor interface recited in claim 9 wherein the main memory interface comprises:

a microprocessor/main memory interface control section adapted to provide control signals between such section and the microprocessor and between such section and the controller; and

a main memory controller, such controller being configured in accordance with the selected one of the plurality of memory types to provide the proper memory protocol to data being transferred between the microprocessor and the main memory through the main memory interface.

13. The microprocessor interface recited in claim 9 wherein the main memory interface comprises:

a microprocessor/main memory interface control section adapted to provide control signals between such section and the microprocessor and between such section and the controller; and

a main memory controller, such controller being configured in accordance with a control signal provided thereto by the microprocessor to address a selected one of the plurality of potential memory capacities, the control signal supplied by the microprocessor indicating to the main memory controller the particular one of the plurality of potential memory capacities of the main memory.

14. The microprocessor interface recited in claim 13 wherein the main memory interface comprises:

a microprocessor/main memory interface control section adapted to provide control signals between such section and the microprocessor and between such section and the controller; and

a main memory controller, such controller being configured in accordance with the selected one of the plurality of memory types to provide a proper memory protocol to data being transferred between the microprocessor and the main memory through the main memory interface.

15. The microprocessor interface recited in claim 14 wherein one main memory type is an SDRAM.

16. The microprocessor interface recited in claim 14 wherein one main memory type is a RDRAM.

17. The microprocessor interface recited in claim 14 wherein the main memory interface includes an error correction and detection unit coupled between the distributor and the main memory controller.

18. The microprocessor interface recited in claim 17 wherein the microprocessor is a Power PC microprocessor.

19. The microprocessor interface recited in claim 5 including a mask to transform the address to an address in the second section of the memory.